IN THE CLAIMS

Please cancel claims 8 and 13 without prejudice.

Please amend claims 7, 9-12 and 14-15. Non-amended claims are included for the convenience of the Examiner.

1. (Original) A memory device comprising:

a first subarray of memory cells organized into rows and columns;

a first plurality of bit lines, each coupled to a column of memory cells;

a first set of subarray isolators to selectively couple the first plurality of bit lines to a first row of sense amplifiers;

a first set of common isolators to selectively couple the first row of sense amplifiers to a plurality of global I/O lines; and

isolator control logic to coordinate the operation of the first set of subarray isolators to allow data in a row of memory cells within the first subarray to be copied to and latched by the first row of sense amplifiers, to coordinate the operation of the first set of common isolators to allow data latched by the first row of sense amplifiers to be transmitted to the plurality of global I/O lines, and to coordinate the operation of the first set of subarray isolators to prevent the loss of data latched by the first row of sense amplifiers by a precharge operation carried out to precharge the first plurality of bit lines.

2. (Original) The memory device of claim 1, further comprising:

a second subarray of memory cells organized into rows and columns;

a second plurality of bit lines, each one of the second plurality of bit lines being coupled to a column of memory cells;

a second set of subarray isolators to selectively couple the second plurality of bit lines to a second row of sense amplifiers, wherein the second set of subarray isolators are operable by the

isolator control logic to allow data in a row within the second subarray to be copied to and latched by the second row of sense amplifiers; and

a second set of common isolators to selectively couple the second row of sense amplifiers to the plurality of global I/O lines, wherein the second set of common isolators is operable by the isolator control logic to allow data latched by the second row of sense amplifiers to be transmitted to the plurality of global I/O lines and to prevent data latched by the second row of sense amplifiers from being lost when the first set of common isolators is operated by the isolator control logic to allow data latched in the first row of sense amplifiers to be transmitted to the plurality of global I/O lines.

3. (Original) The memory device of claim 1, further comprising:

a first bank of memory comprised of the first and second subarrays, the first and second set of subarray isolators, the first and second set of sense amplifiers, and the first and second sets of common isolators; and

a second bank of memory.

4. (Original) The memory device of claim 1, further comprising control logic configured to receive a read command wherein data is copied from a row within the first subarray through both the first plurality of bit lines and the first set of subarray isolators to the first row of sense amplifiers where the data is latched, and the data latched within the first row of sense amplifiers is transmitted through the first set of common isolators to the plurality of global I/O lines.

5. (Original) The memory device of claim 4, wherein the control logic is further configured to receive a mini read command where data has already been copied from a row within the first subarray and latched by the first row of sense amplifiers, and to respond by operating the first set of common isolators to allow the data latched by the first row of sense amplifiers to be

transmitted by the first row of sense amplifiers through the first set of common isolators to the plurality of global I/O lines.

6. (Original) The memory device of claim 5, wherein the control logic is further configured to receive a mini row activate command wherein a row address identifying a row within the first subarray is received by the control logic to signal that data latched within the first row of sense amplifiers from the row within the first subarray is to be transmitted through the first set of common isolators to the plurality of global I/O lines upon receipt of a read command.

7. (Currently Amended) A controlling device comprising:

a first storage location in which data concerning the status of rows within a bank of memory cells within a memory device is stored;

control logic coupled to the first storage location to check data within the first storage location to determine if the contents of a specific row from which data is to be read is already cached by a row of sense amplifiers and to check if the specific row is the open row within the bank; and

a memory bus coupling the control logic to the memory device to allow commands to be transmitted from the control logic to the memory device.~~:~~

~~The controlling device of claim 7,~~ wherein a mini read command is transmitted by the control logic to the memory device if the contents of the specific row are already cached by a row of sense amplifiers and the specific row is the open row within the bank to cause the data cached by the row of sense amplifiers to be output by the memory device.

8. (Canceled)

9. (Currently Amended) A controlling device comprising:

a first storage location in which data concerning the status of rows within a bank of memory cells within a memory device is stored;

control logic coupled to the first storage location to check data within the first storage location to determine if the contents of a specific row from which data is to be read is already cached by a row of sense amplifiers and to check if the specific row is the open row within the bank; and

a memory bus coupling the control logic to the memory device to allow commands to be transmitted from the control logic to the memory device.;

~~The controlling device of claim 7,~~ wherein a mini row activate command and a mini read command are transmitted by the control logic to the memory device if the contents of the specific row are already cached by a row of sense amplifiers, but the specific row is not the open row within the bank, to cause the specific row to become the open row within the bank and to cause the data cached by the row of sense amplifiers to be output by the memory device.

10. (Currently Amended) A controlling device comprising:

a first storage location in which data concerning the status of rows within a bank of memory cells within a memory device is stored;

control logic coupled to the first storage location to check data within the first storage location to determine if the contents of a specific row from which data is to be read is already cached by a row of sense amplifiers and to check if the specific row is the open row within the bank; and

a memory bus coupling the control logic to the memory device to allow commands to be transmitted from the control logic to the memory device.;

~~The controlling device of claim 7,~~ wherein a read command is transmitted by the control logic to the memory device if the contents of the specific row are not already cached by a row of sense amplifiers, but the specific row is the open row within the bank, to cause the contents of the memory cells of the specific row to be copied to a row of sense amplifiers so as to be cached

by the row of sense amplifiers, and to cause the data copied from the specific row and cached by the row of sense amplifiers to be output by the memory device.

11. (Currently Amended) A controlling device comprising:

a first storage location in which data concerning the status of rows within a bank of memory cells within a memory device is stored;

control logic coupled to the first storage location to check data within the first storage location to determine if the contents of a specific row from which data is to be read is already cached by a row of sense amplifiers and to check if the specific row is the open row within the bank; and

a memory bus coupling the control logic to the memory device to allow commands to be transmitted from the control logic to the memory device.;

~~The controlling device of claim 7,~~ wherein a row activate command and a read command are transmitted by the control logic to the memory device if the contents of the specific row are not already cached by a row of sense amplifiers and the specific row is not the open row within the bank to cause the specific row to become the open row of the bank and be made ready for a read operation, and to cause the contents of the memory cells of the specific row to be copied to a row of sense amplifiers so as to be cached by the row of sense amplifiers, and to cause the data copied from the specific row and cached by the row of sense amplifiers to be output by the memory device.

12. (Currently Amended) A computer system comprising:

a processor;

a memory device having at least one bank in which a plurality of memory cells are organized into rows;

a memory controller coupled to the processor and having a first storage location that the memory controller accesses to determine if the contents of a specific row from which data is to

be read in response to a request for data from the processor is already cached by a row of sense amplifiers, and to check if the specific row is the open row within the bank; and

a memory bus coupling the control logic to the memory device to allow commands to be transmitted from the control logic to the memory device.;

~~The computer system of claim 12,~~ wherein the control logic transmits a mini read command to the memory device if the contents of the specific row from which the processor has requested data are already cached by a row of sense amplifiers and the specific row is the open row within the bank to cause the data cached by the row of sense amplifiers to be output by the memory device.

13. (Canceled)

14. (Currently Amended) A computer system comprising:

a processor;

a memory device having at least one bank in which a plurality of memory cells are organized into rows;

a memory controller coupled to the processor and having a first storage location that the memory controller accesses to determine if the contents of a specific row from which data is to be read in response to a request for data from the processor is already cached by a row of sense amplifiers, and to check if the specific row is the open row within the bank; and

a memory bus coupling the control logic to the memory device to allow commands to be transmitted from the control logic to the memory device.;

~~The computer system of claim 12,~~ wherein the control logic transmits a mini row activate command and a mini read command to the memory device if the contents of the specific row from which the processor has requested data are already cached by a row of sense amplifiers, but the specific row is not the open row within the bank, to cause the specific row to become the

open row within the bank and to cause the data cached by the row of sense amplifiers to be output by the memory device.

15. (Currently Amended) A computer system comprising:

a processor;

a memory device having at least one bank in which a plurality of memory cells are organized into rows;

a memory controller coupled to the processor and having a first storage location that the memory controller accesses to determine if the contents of a specific row from which data is to be read in response to a request for data from the processor is already cached by a row of sense amplifiers, and to check if the specific row is the open row within the bank; and

a memory bus coupling the control logic to the memory device to allow commands to be transmitted from the control logic to the memory device.:

~~The computer system of claim 12,~~ wherein the control logic transmits a row activate command and a read command to the memory device if the contents of the specific row from which the processor has requested data are not already cached by a row of sense amplifiers and the specific row is not the open row within the bank to cause the specific row to become the open row of the bank and be made ready for a read operation, and to cause the contents of the memory cells of the specific row to be copied to a row of sense amplifiers so as to be cached by the row of sense amplifiers, and to cause the data copied from the specific row and cached by the row of sense amplifiers to be output by the memory device.

16. (Original) A method comprising:

determining whether or not the contents of a specific row of memory cells within a subarray of memory cells organized into multiple rows and columns are already cached within a row of sense amplifiers;

determining whether or not the specific row of memory cells is the open row of a bank of a memory device in which the subarray is located;

transmitting a mini read command to the memory device to read from the row of sense amplifiers a portion of the contents of the specific row of memory copied to the row of sense amplifiers if the contents of the specific row have been copied to the row of sense amplifiers and the specific row is the open row of the bank of the memory device; and

receiving the portion of the contents of the specific row of memory.

17. (Original) The method of claim 16, further comprising transmitting a mini row activate command to the memory device cause the specific row to become the open row of the banks of the memory device if the contents of the specific row have been copied to the row of sense amplifiers, but the specific row is not the open row of the bank of the memory device.

18. (Original) The method of claim 16, further comprising transmitting a row activate command to the memory device to make the specific row the open row of the bank of the memory device, waiting for the row activate command to complete, transmitting a read command to the memory device to cause a set of isolators to permit the contents of the specific row to be copied to the row of sense amplifiers and to read from the row of sense amplifiers a portion of the contents of the specific row.

19. (Original) A method comprising:

operating a first set of isolators coupled to a first row of sense amplifiers in response to the receipt of a mini read command to allow data copied into the first row of sense amplifiers from a first row of memory cells of a first subarray to be output by the first row sense amplifiers through the first set of isolators to a set of global I/O lines that further couple the first row of sense amplifiers through the set of global I/O lines to an output of a memory device of which the subarray is a part; and

operating a second set of isolators coupled between a first set of bit lines and the first row of sense amplifiers in response to the receipt of a precharge command to isolate the first row of sense amplifiers from the first set of bit lines while a precharge operation to precharge the first set of bit lines is carried out so as to prevent data cached by the first row of sense amplifiers from being lost.

20. (Original) The method of claim 19, further comprising operating the first set of isolators to isolate the first row of sense amplifiers from the set of global I/O lines while allowing the second row of sense amplifiers caching data copied from a second row of memory cells to be coupled through the set of global I/O lines to the output of the memory device and to transmit data from within the second row of sense amplifiers to the output of the memory device without data stored within the first row of sense amplifiers being lost.

21. (Original) A machine-accessible medium comprising code that when executed by a processor within an electronic device, causes the electronic device to:

check whether or not a memory device is capable of caching the contents of a row of memory cells within a row of sense amplifiers;

program a memory controller to transmit a mini row activate command to activate a row of which the contents have been determined to have been cached within a row of sense amplifiers to make possible the subsequent reading of the data from the row of sense amplifiers; and

program a memory controller to transmit a mini read command to read data cached within the row of sense amplifiers in lieu of reading the data directly from the row of memory cells being cached by the row of sense amplifiers.

22. (Original) The machine-accessible medium of claim 21, further causing the electronic device to transmit a precharge command causing the row of sense amplifiers to be isolated from

bit lines that otherwise couple the row of sense amplifiers to columns of memory cells within a subarray while the precharge operation to precharge the bit lines is carried out so as to prevent data cached within the row of sense amplifiers from being lost.